

KOREAN PATENT ABSTRACTS

(11)Publication number: 1020020067769 A
(43)Date of publication of application: 24.08.2002

(21)Application number: 1020010008099
(22)Date of filing: 19.02.2001
(51)Int. Cl: H03M 13/37

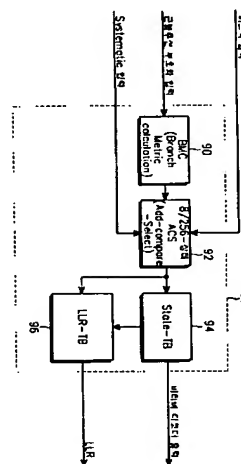
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(54) INTEGRATED DECODER OF VITERBI DECODER AND TURBO DECODER AND METHOD FOR PERFORMING INTEGRATED DECODING PROCESS

(57) Abstract:

PURPOSE: An integrated decoder of a Viterbi decoder and a turbo decoder and a method for performing an integrated decoding process are provided to reduce complexity of a hardware and economize a memory source by forming a Viterbi decoder and a turbo decoder with one body.

CONSTITUTION: An 8-state SOVA/256-state Viterbi decoder(80) is formed by including a hard decision Viterbi decoder in a SOVA decoder of a turbo decoder. The 8-state SOVA/256-state Viterbi decoder(80) has an integrated structure of the 8-state SOVA decoder and the Viterbi decoder. In a Viterbi decoder mode, the 8-state SOVA/256-state Viterbi decoder(80) transmits an output to an output terminal since 8-state SOVA/256-state Viterbi decoder (80) does not use necessary parts used in a repetition decoding process of the turbo decoder. In a turbo decoding mode, the repetition decoding process is performed by processing 8 states at once.

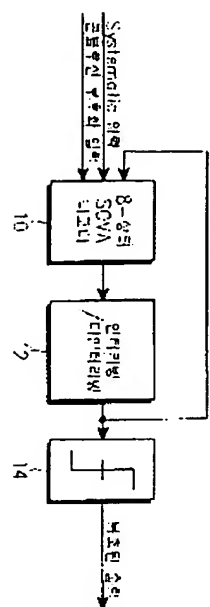


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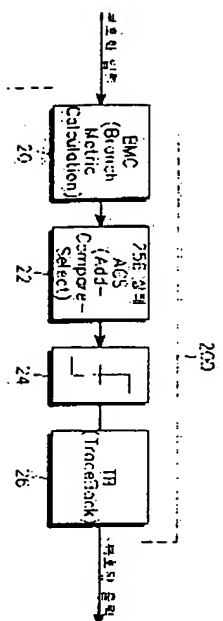
Legal Status

Date of final disposal of an application (20031129)
Patent registration number (1004151160000)
Date of registration (20031230)
Number of opposition against the grant of a patent ()
Date of opposition against the grant of a patent (00000000)
Number of trial against decision to refuse ()
Date of requesting trial against decision to refuse ()
Date of extinction of right ()

도면 1



도면 2



도면 3

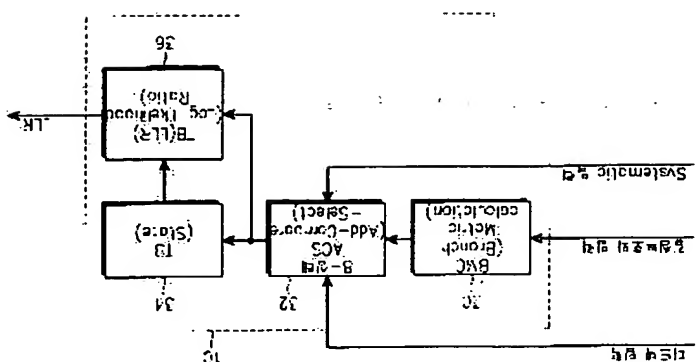


FIG. 4

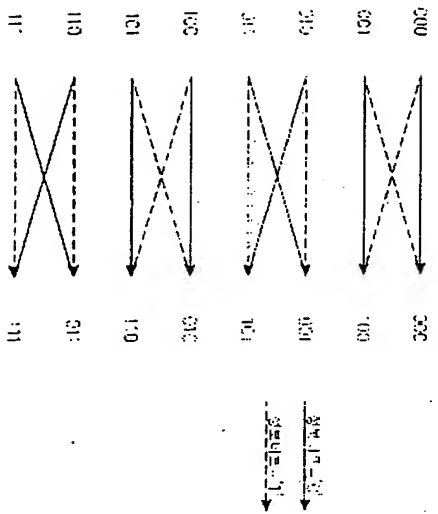


FIG. 5

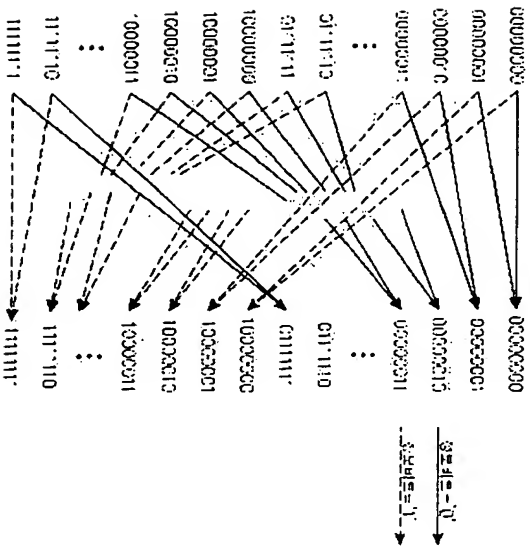
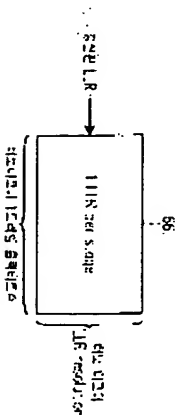
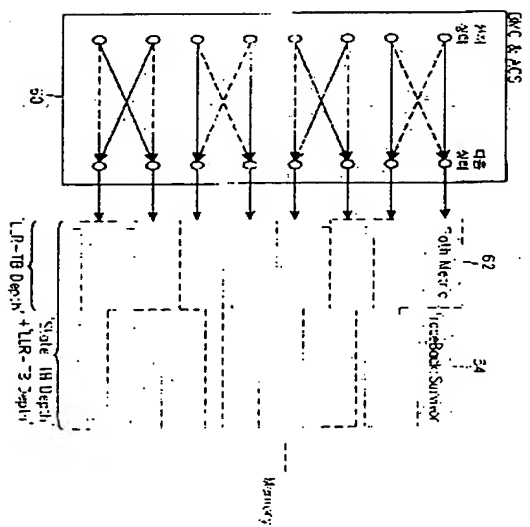
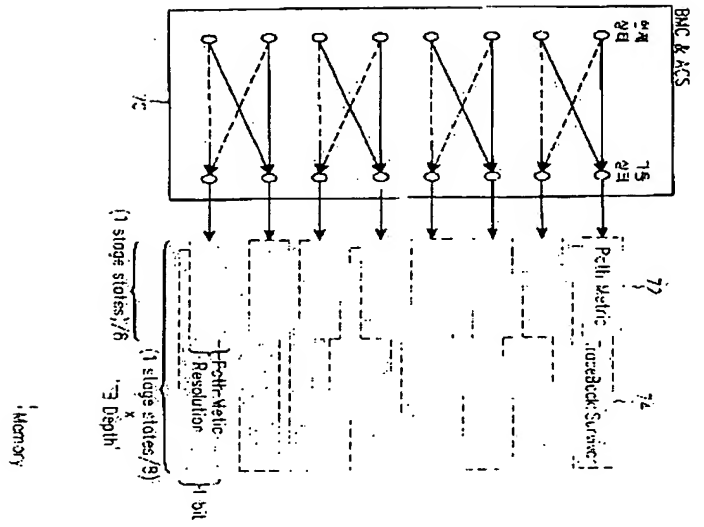


FIG. 6

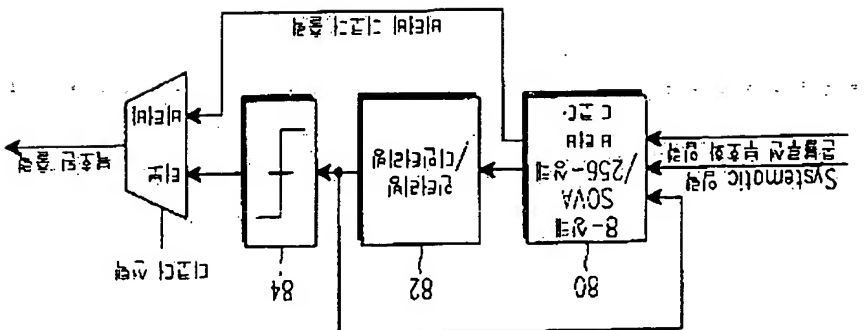


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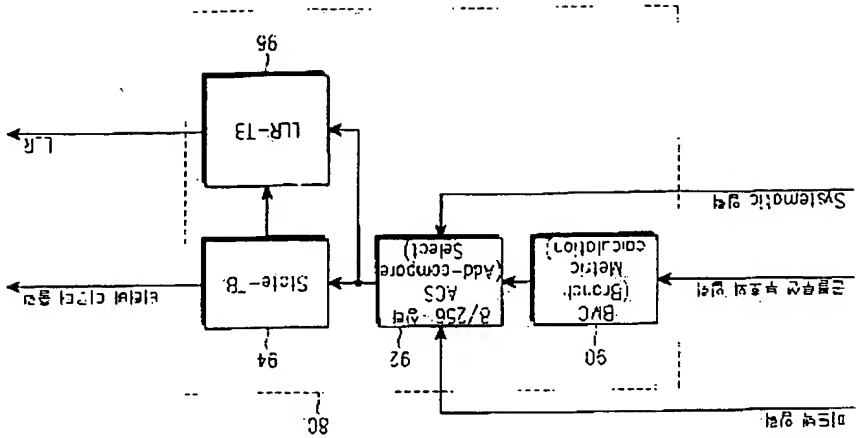
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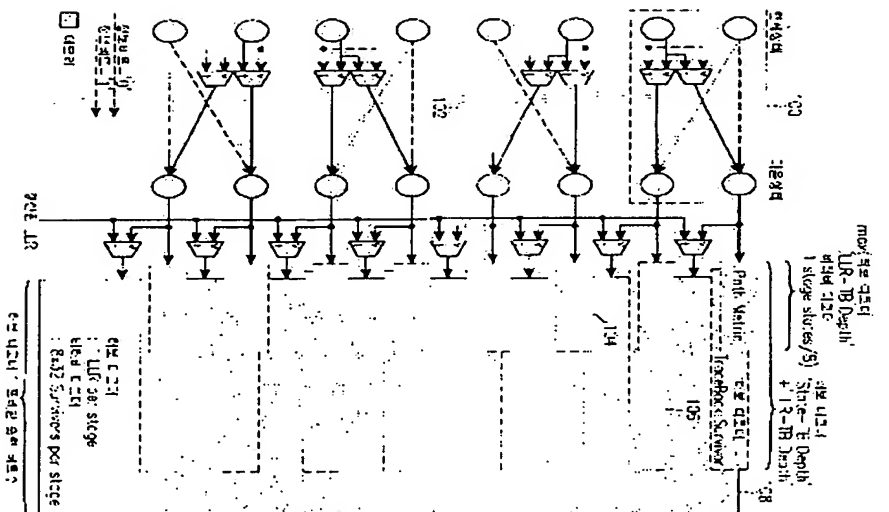
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